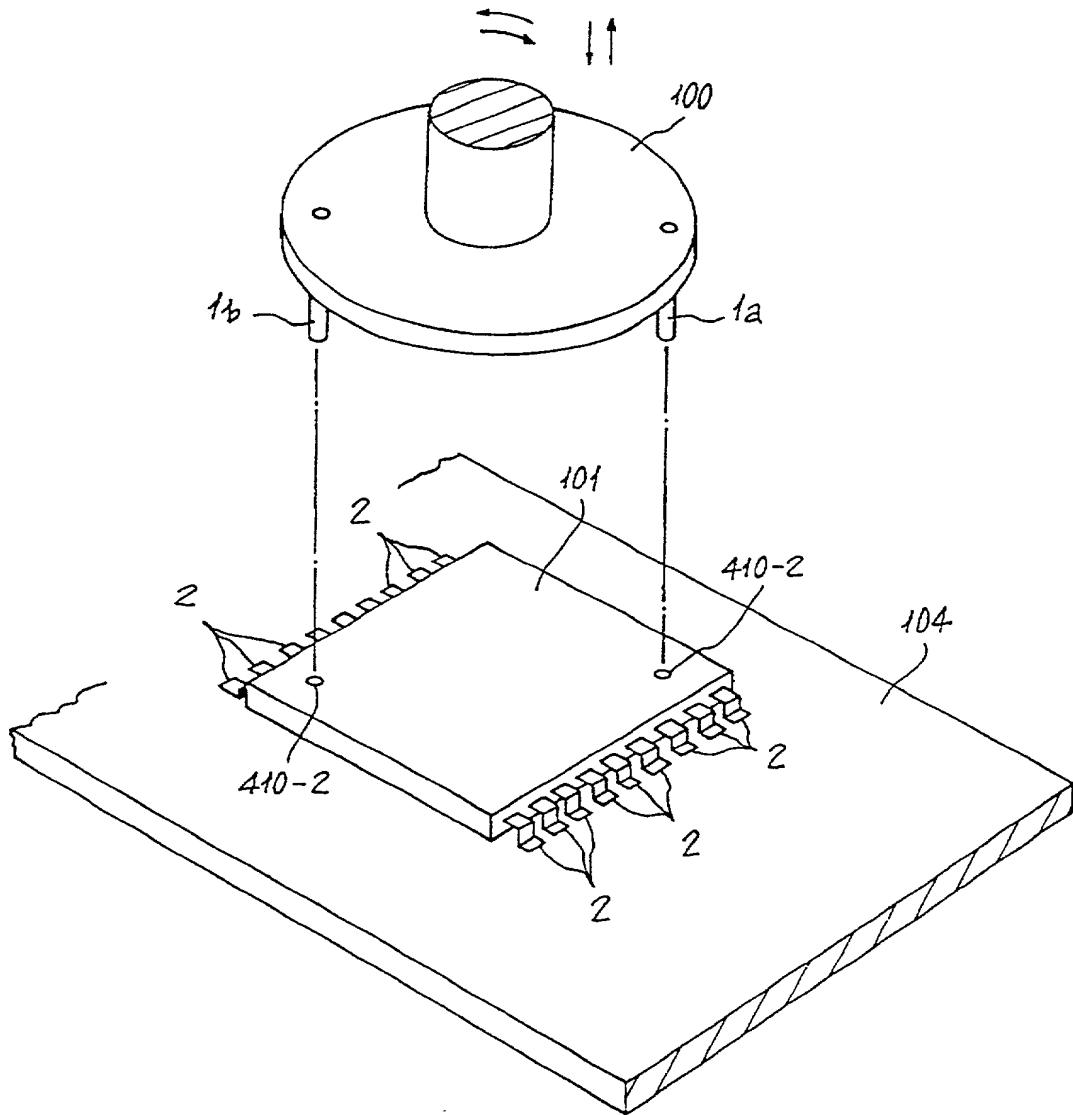


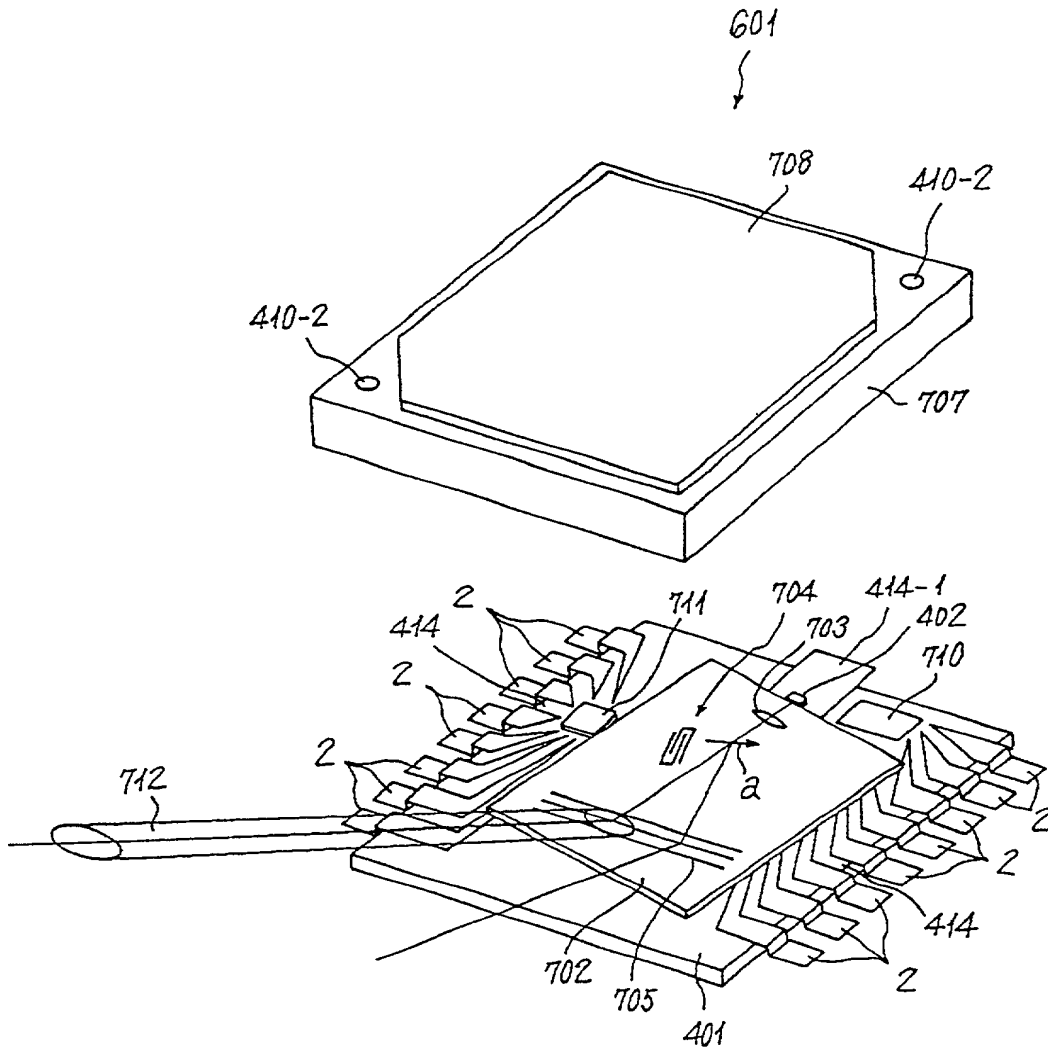
3/27

FIG. 3



4/27

FIG. 4



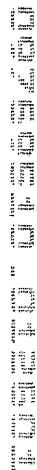


FIG. 6

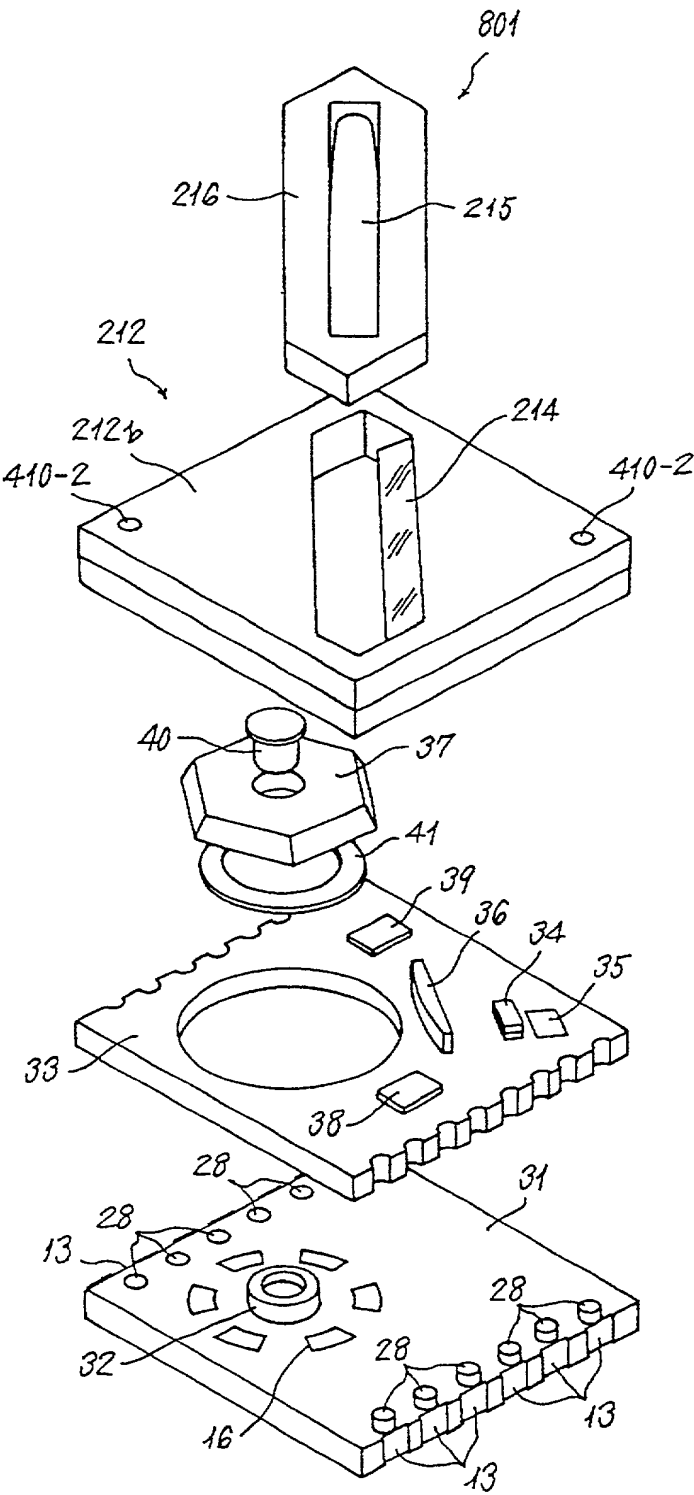
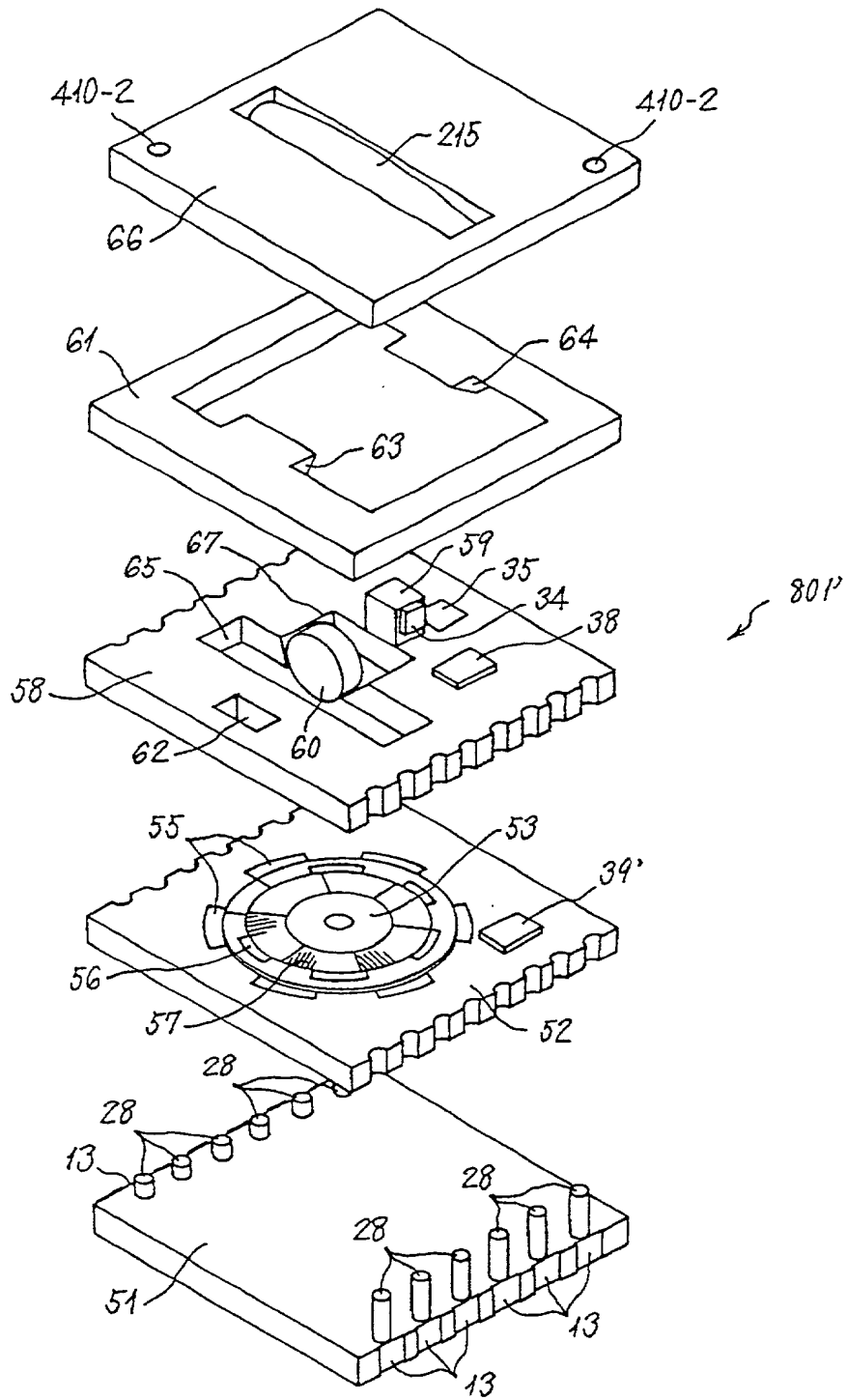


FIG. 1 is a cross-sectional view of a semiconductor device 801. The device includes a substrate 33. A top layer 34 is formed on the substrate. A central region of the device contains a stack of layers. The stack includes a layer 212, which is further divided into sub-layers 212a and 212b. Above layer 212 is layer 214, followed by layer 215, and then layer 216. Below layer 212 is layer 217. Other layers in the stack include 31, 35, 36, 37, 40, and 41. An arrow points to the central stack area.

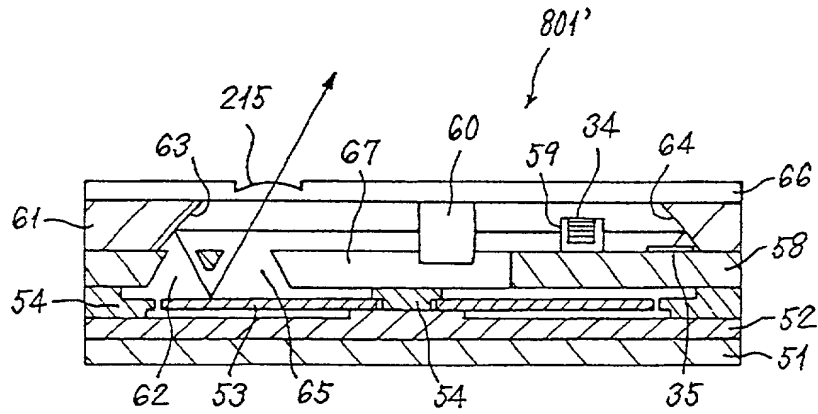
8/27

FIG. 8



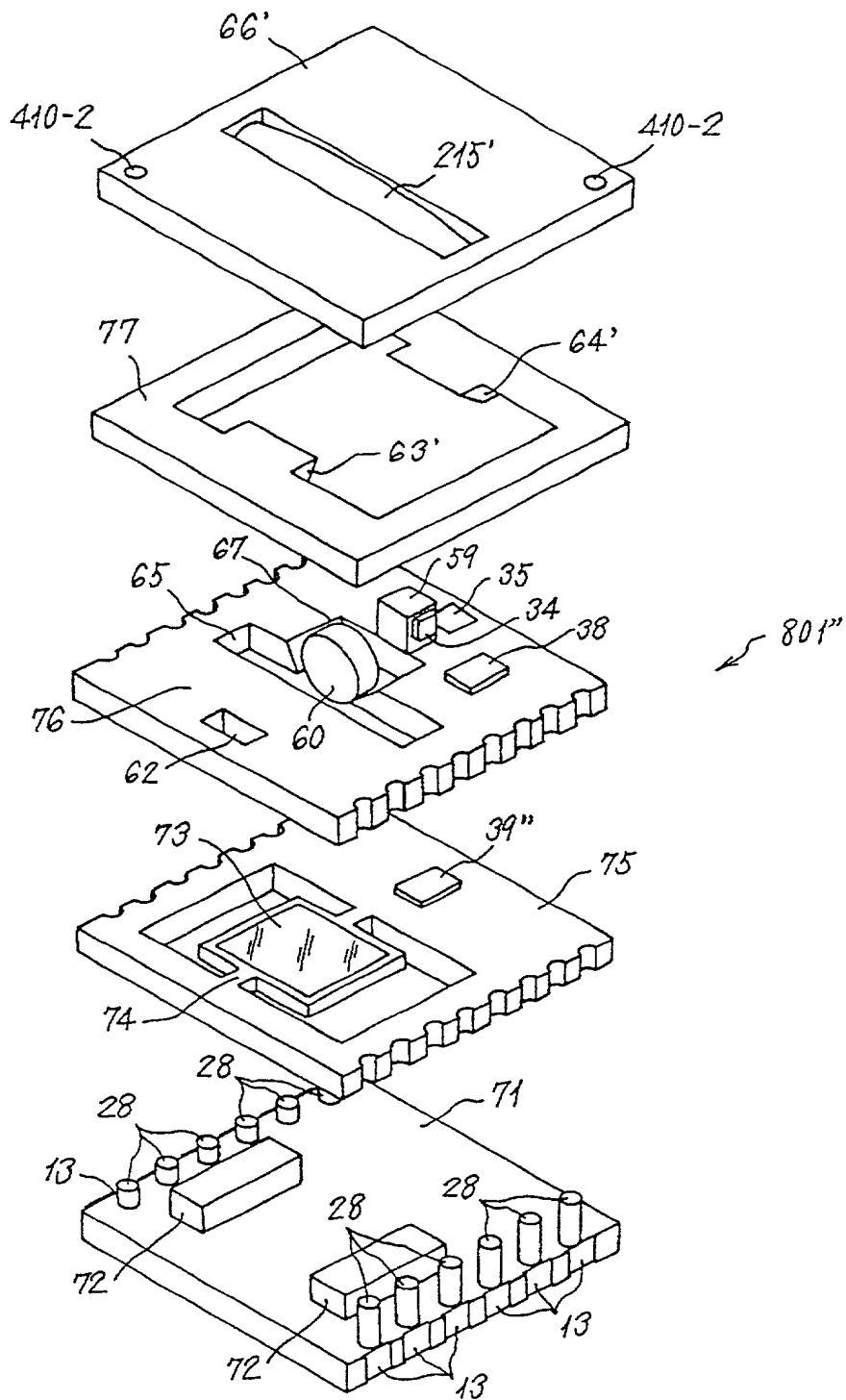
9/27

FIG. 9



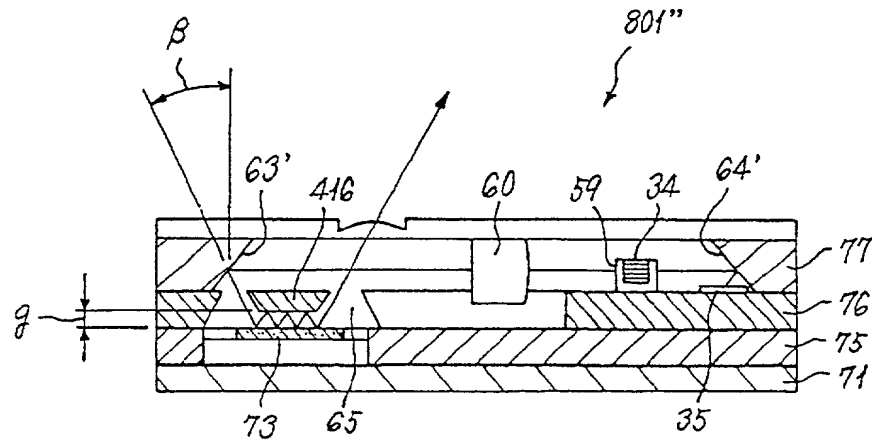
10/27

FIG. 10



11/27

FIG. 11



12/27

FIG. 12

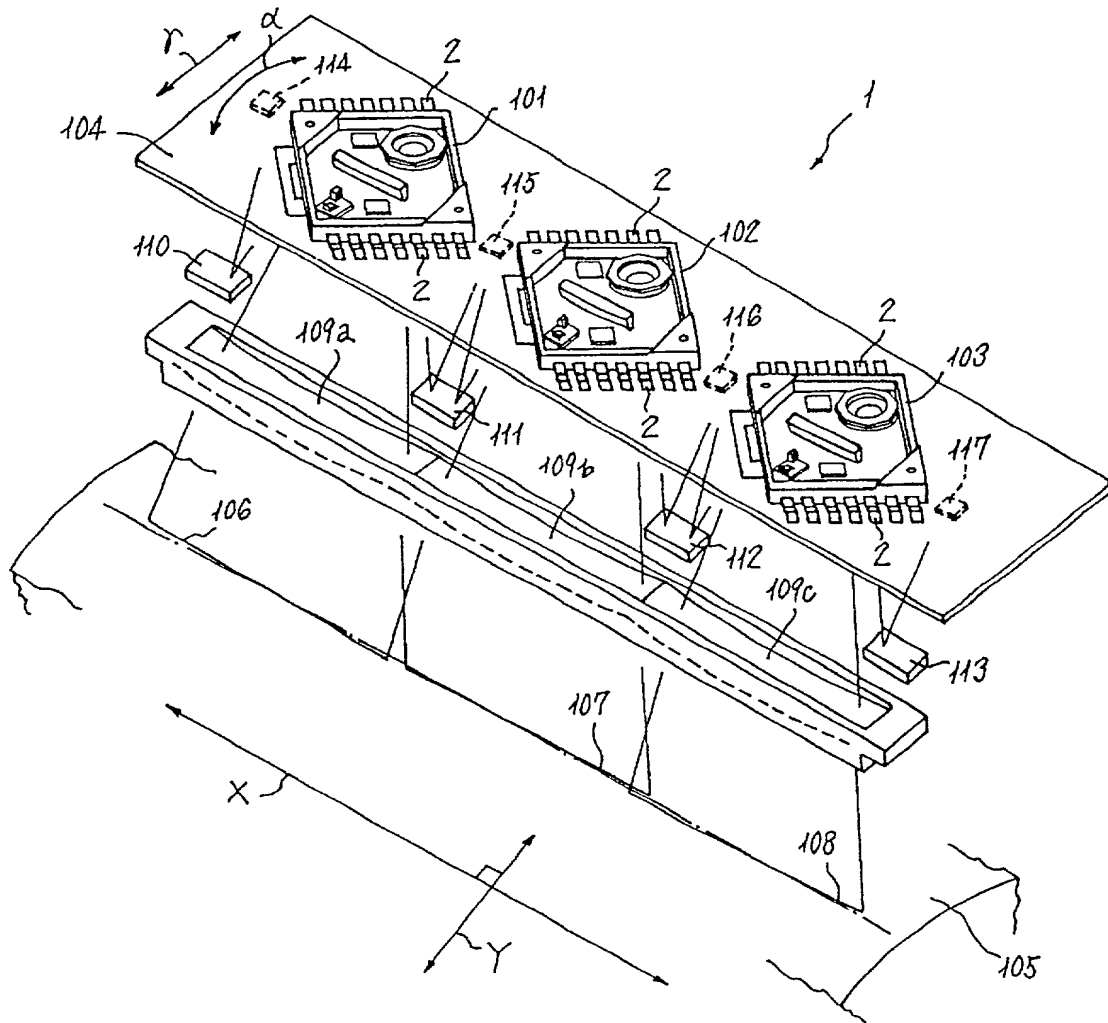
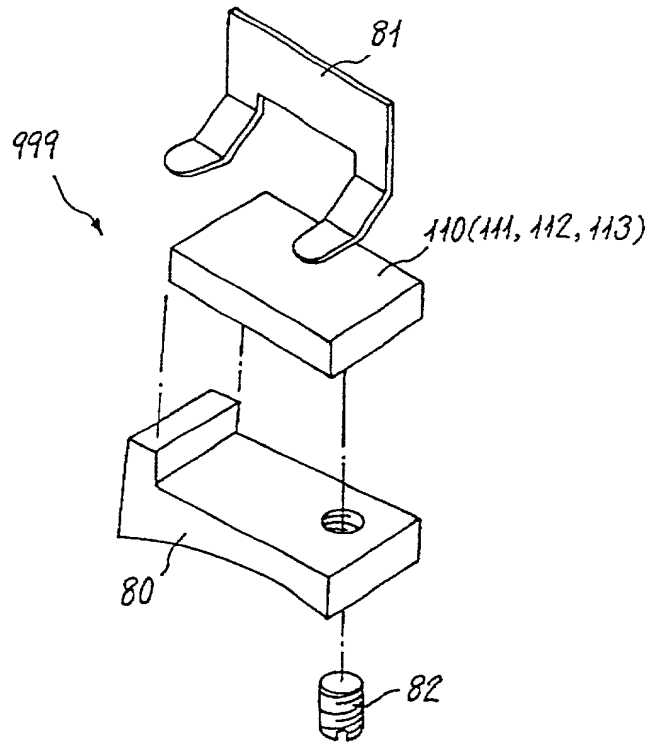


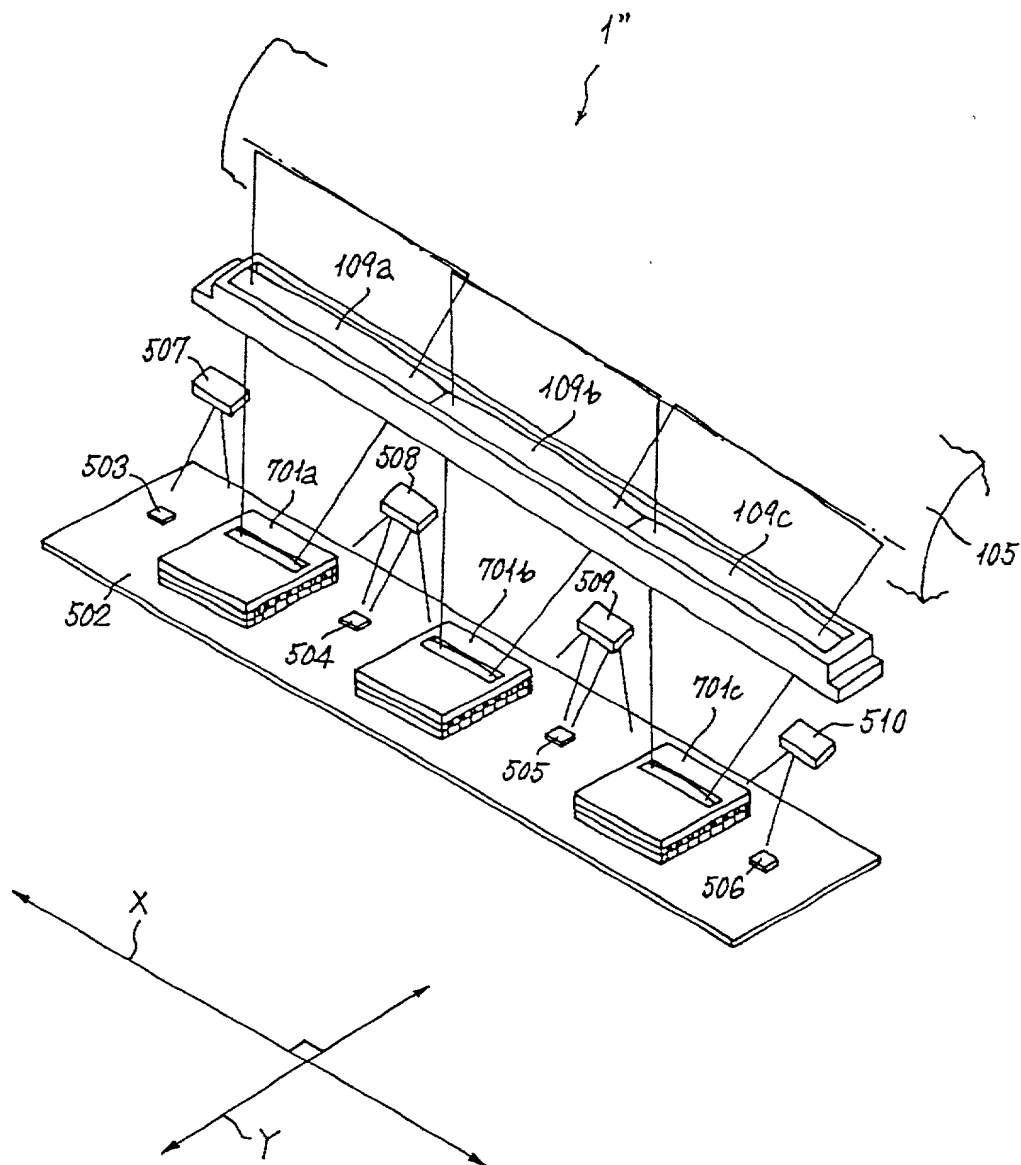
FIG. 13



[illegible]

15/27

FIG. 15



16/27

FIG.16

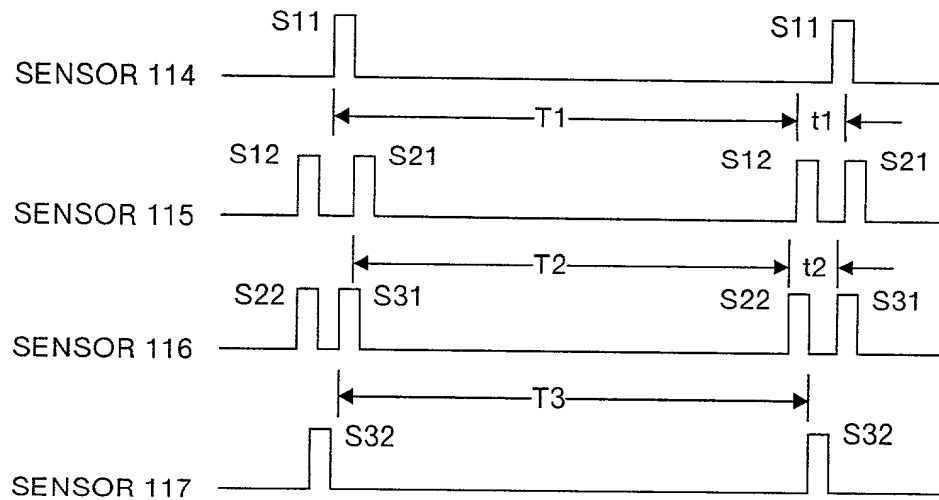
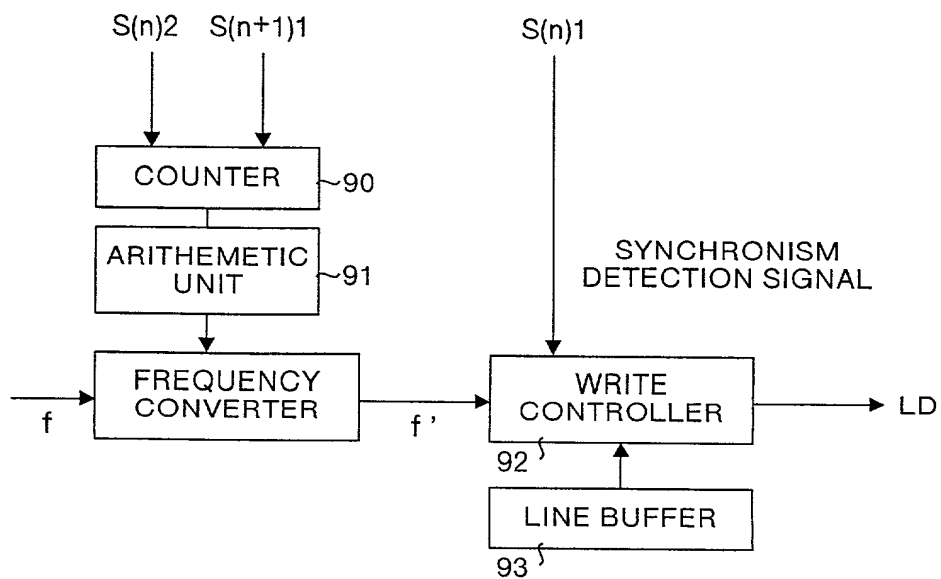
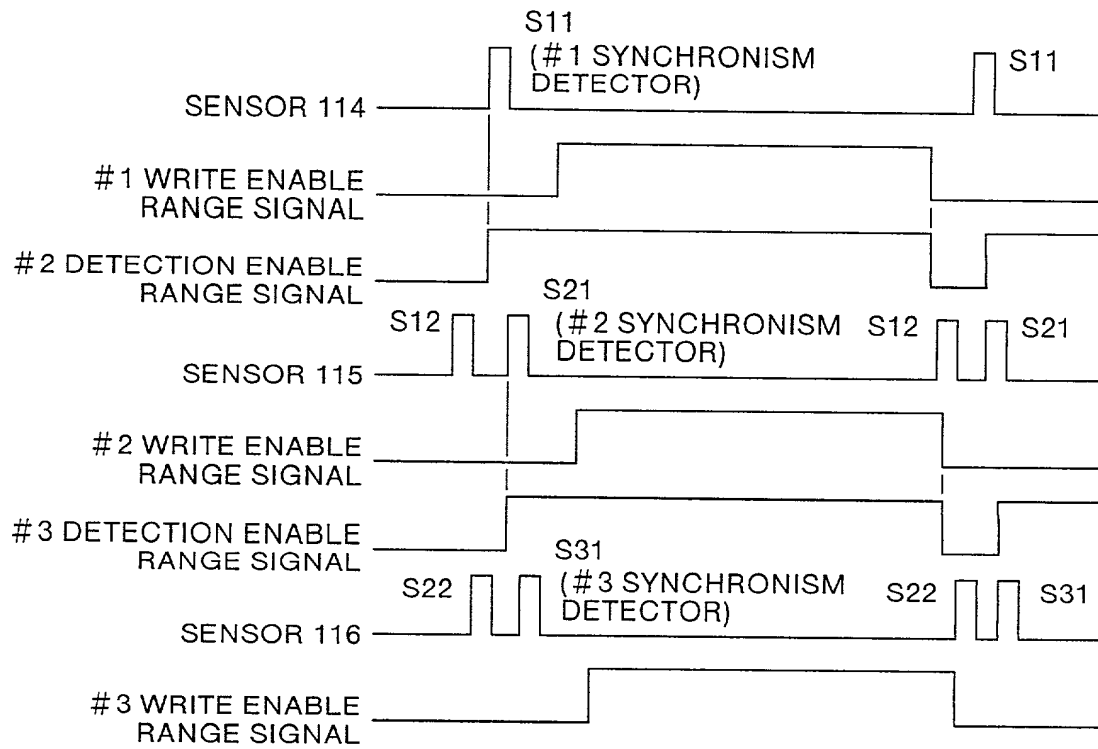


FIG.17



17/27

FIG.18



#1 : OPTICAL SCAN MODULE 101
#2 : OPTICAL SCAN MODULE 102
#3 : OPTICAL SCAN MODULE 103

18/27

FIG.19

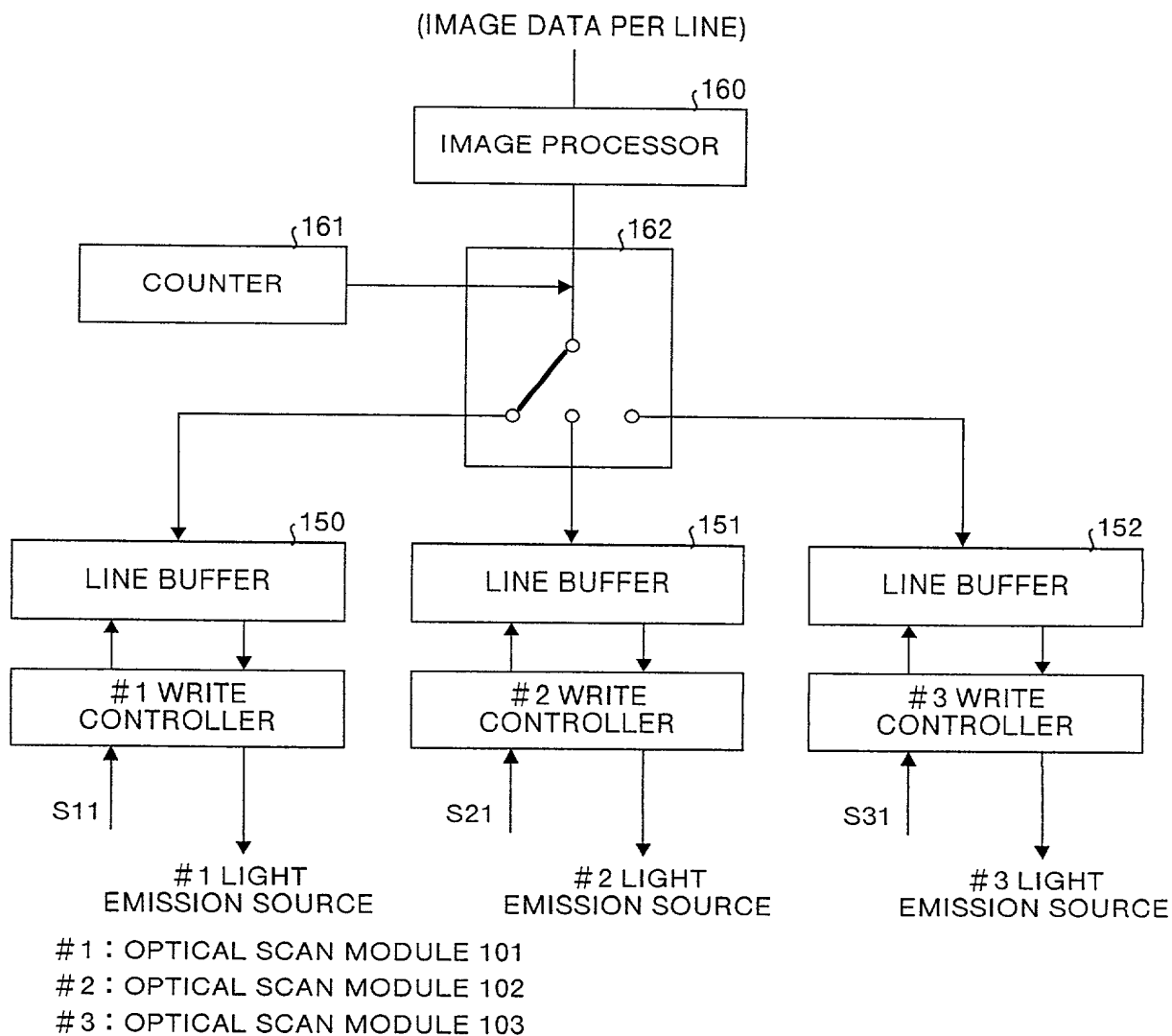
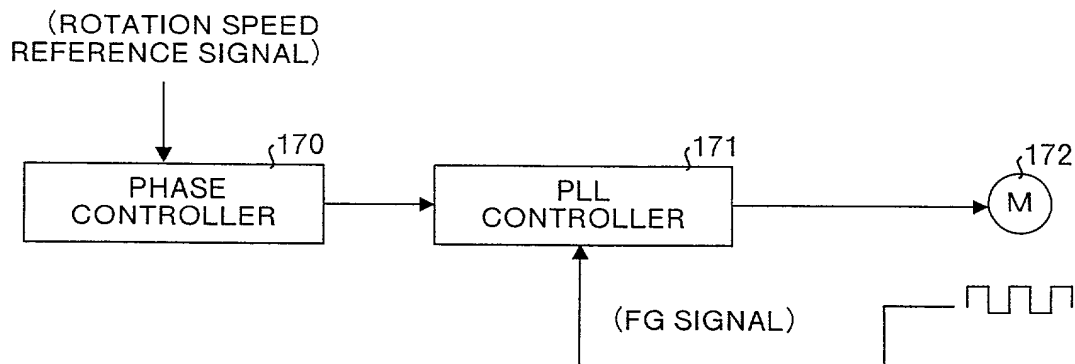
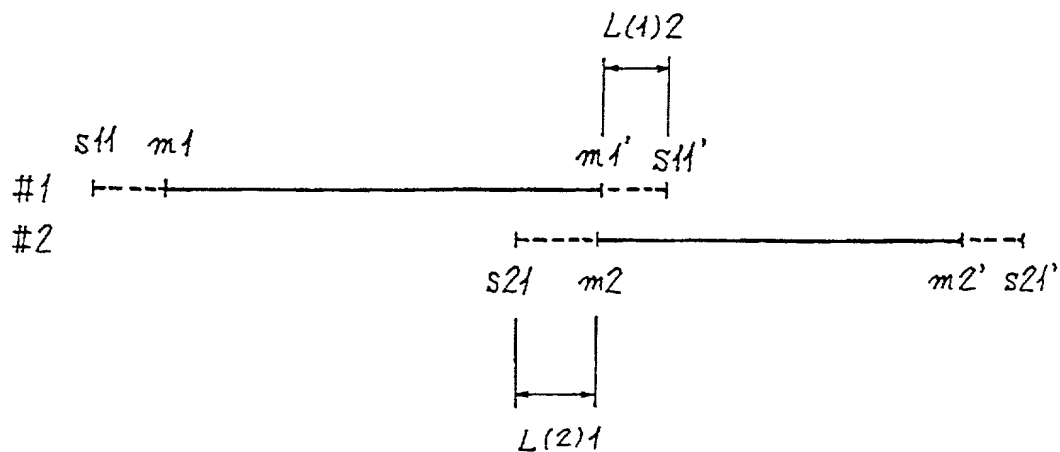


FIG.20



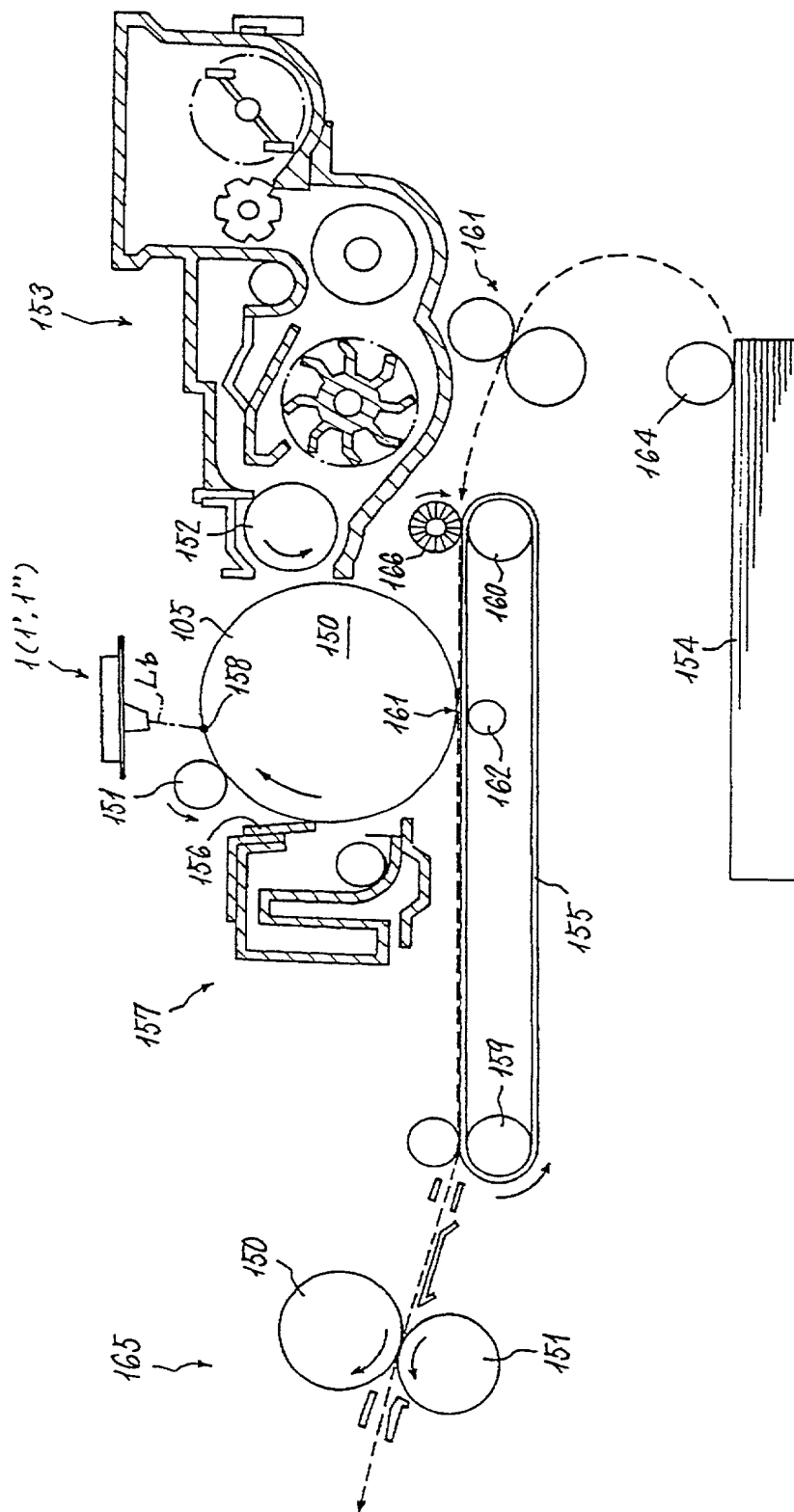
19/27

FIG. 21



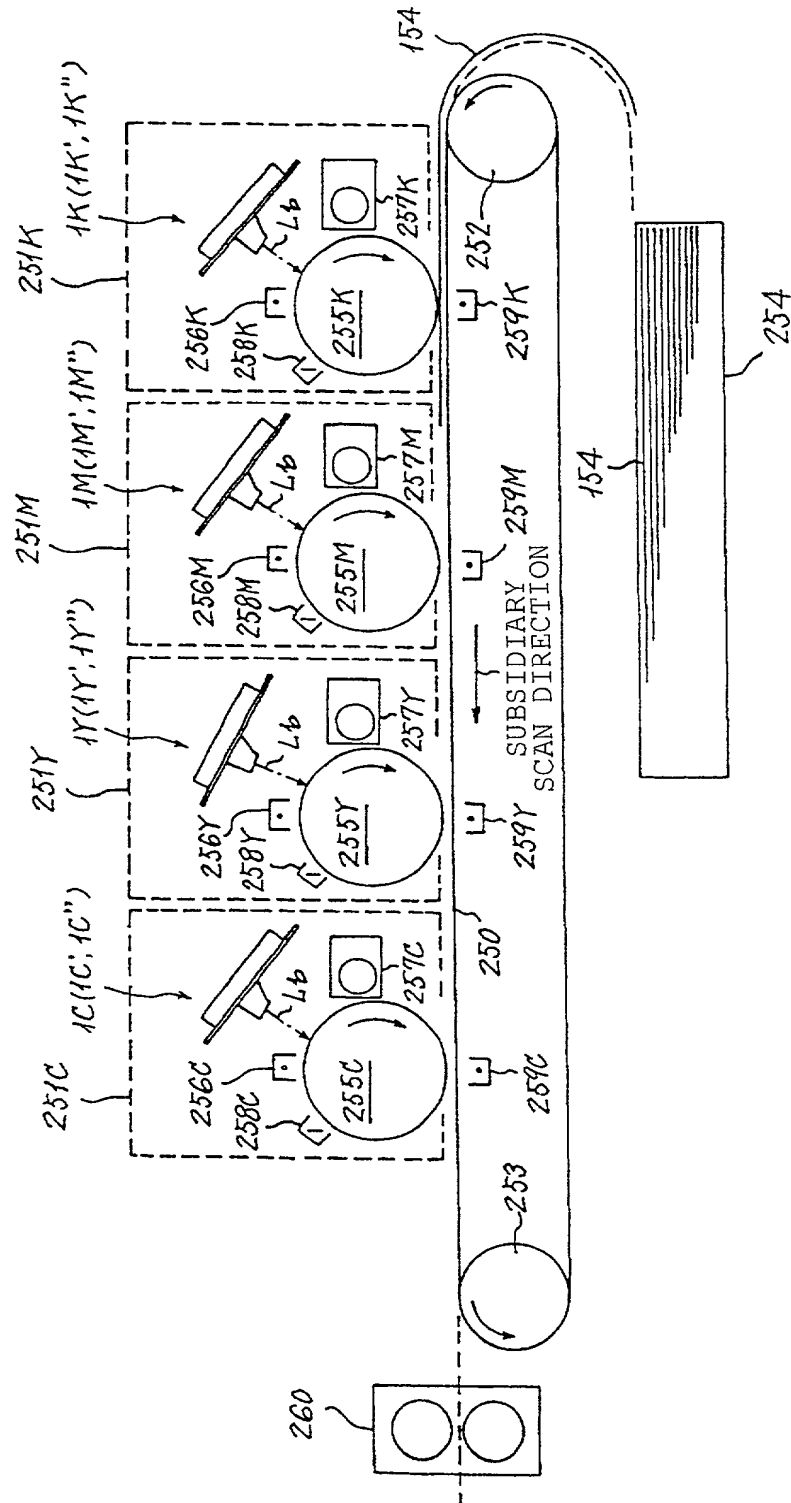
20/27

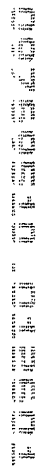
FIG. 22



21/27

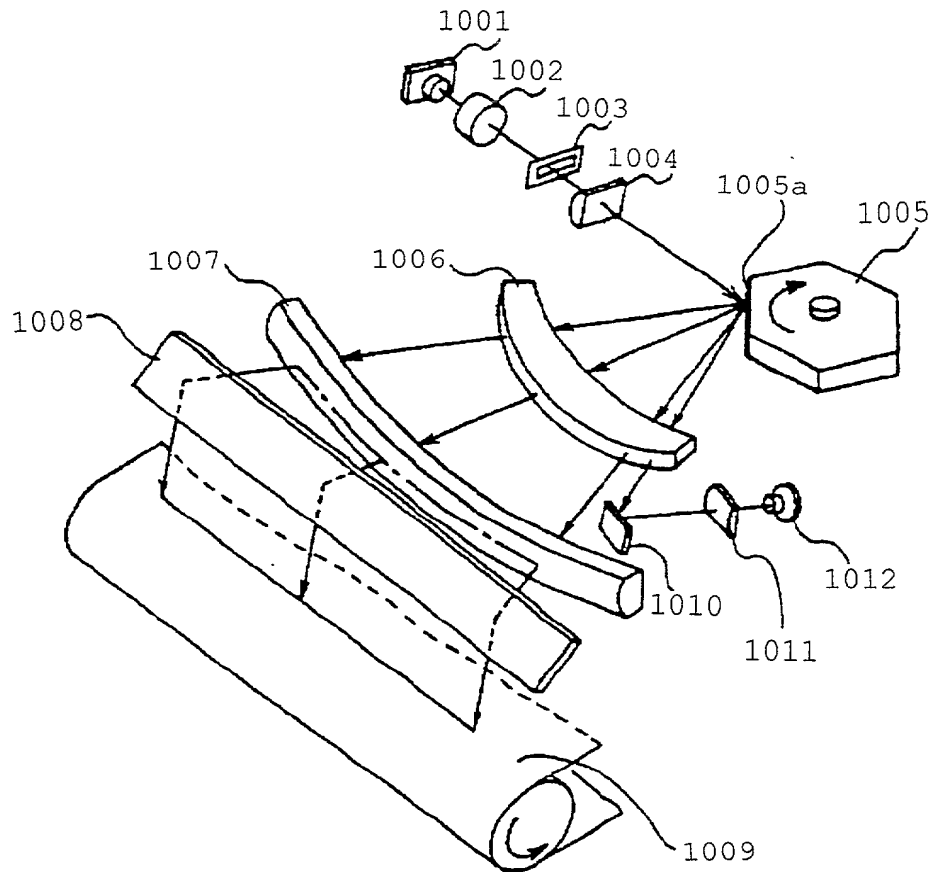
FIG. 23



[illegible]

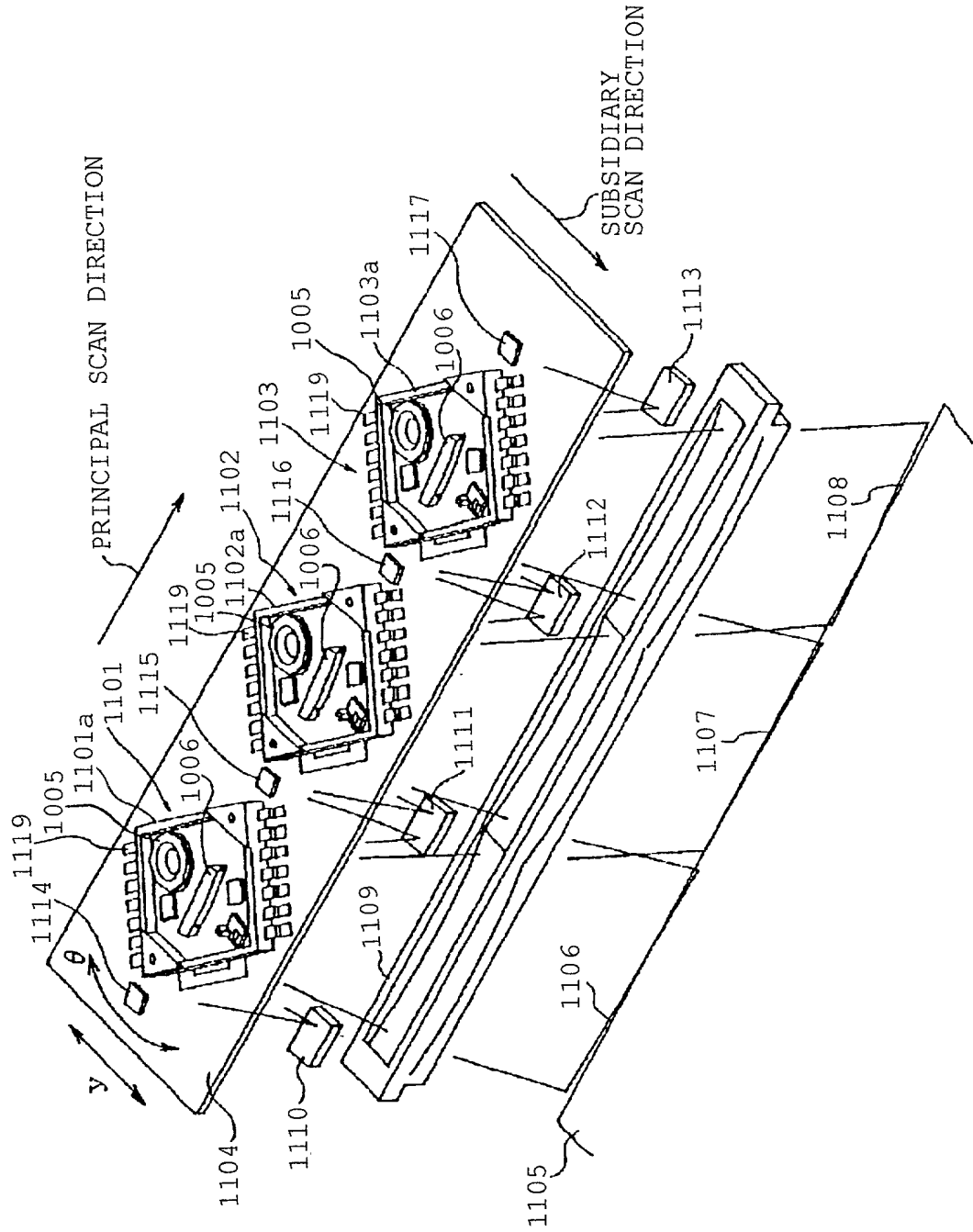
24/27

FIG. 26



25/27

FIG. 27



26/27

FIG. 28

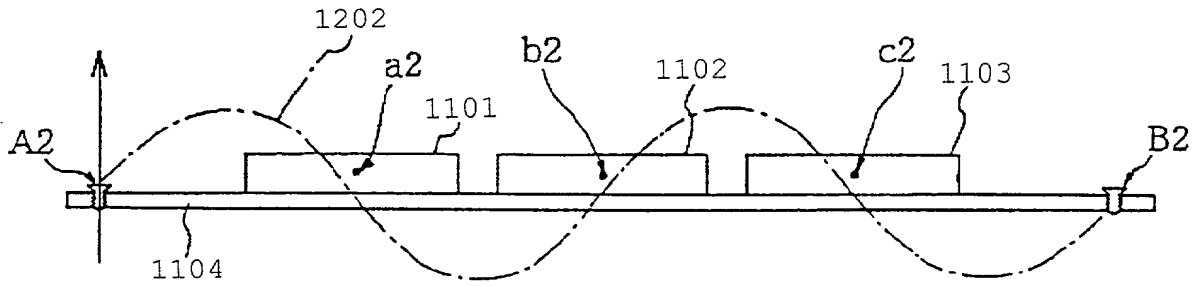


FIG. 29

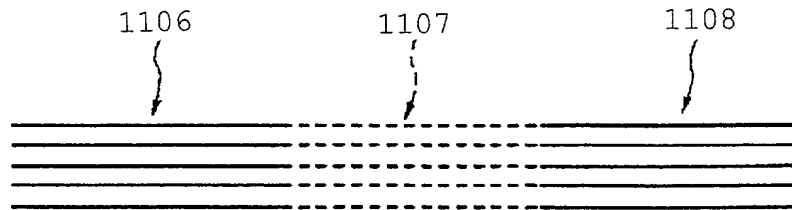
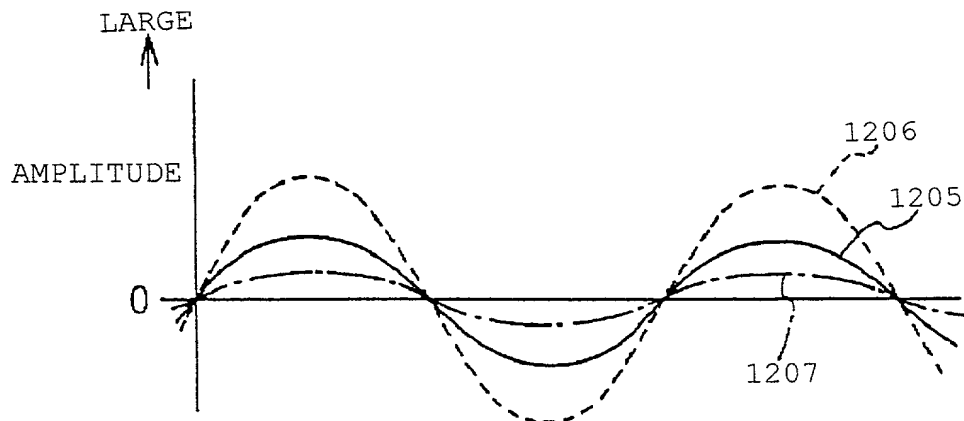


FIG. 30



27/27

FIG. 31

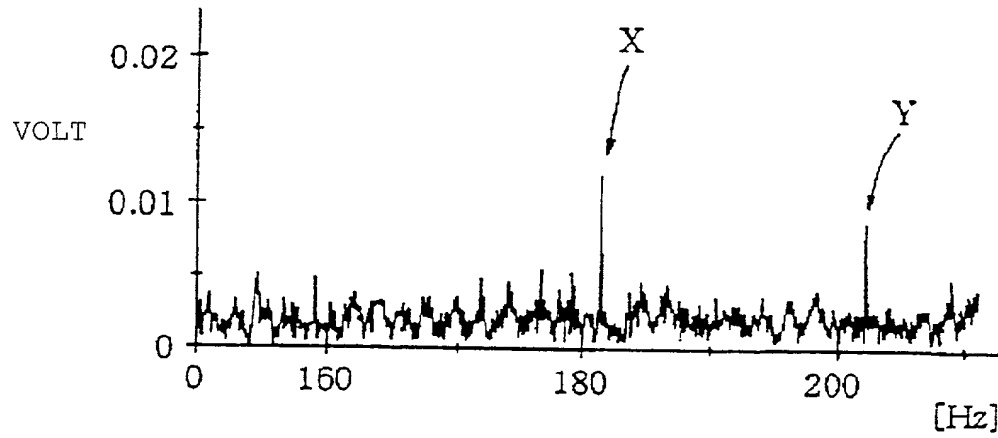


FIG. 32

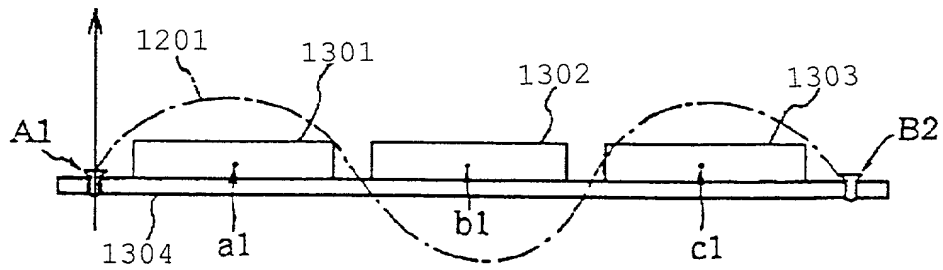


FIG. 33

